SRAM Write up

Bhavnagarwala

The motivation of this paper is to provide a higher cell voltage to the cell without providing an additional voltage source and the metal for this network. The increased voltage is provided by bootstrapping. Through alternating powerlines and bitlines and placing PMOS pass gates on the powerlines controlled by the wordline, the powerlines are allowed to float. The effective voltage is boosted by the transition, thus improving beta and cell read current. , This improved SNM by 18% with a less than 13% area penalty. There were concerns regarding the ability to control the boost in the powerlines, due to its dependency on timing and the oass gates and its implementability.

Kellah08

The motivation for this paper is finding ways to deal with variations in process, variation, and temperature to utilize the wordline under drive read assist method. To deal with PVT, the paper utilizes a series resistor network , which uses a transistor to take variation into account to adjust the voltage the wordline is driven to. The paper also introduces the p-cell which uses PMOS transistors as access transistors to improve beta and dynamic voltage to improve the write stability. Through those improvements, they receive decent improvements for the area overhead. There is confusion on some of the graphs on page two of this paper, not distinguish between margins.

Pilo

The motivation for this paper is reducing the number of read failures due to variation. Pilo does this by reading all bitcells on the selected line through a sense amp and then fully swinging the bitline. The method is successful as long as the sense amp is not enabled too aggressively and adds only a 4% area overhead to the circuits. Some limitations of this paper are that they size their PMOS weak to ensure they get bit failures and that a large amount of charge is wasted by discharging the bitlines and recharging the bitlines.

Abu-Rahma

The motivations for this paper is to present a lower energy, faster SRAM read assist method. This is done through selective precharge. The bitlines and sense amp lines are separated by a switch and are precharged and predischarged respectively. The switches are closed and charge sharing occurs, thus charge sharing between the two lines and reducing the voltage on the bitline. The read occurs when the switch on the selected column remains closed and the others are

opened. The paper claims this method is faster because the sense amp can be enabled at a lower voltage delta due to the lower voltage on BL and BLB. The weaknesses of this method are the unnecessary charge dissipation and rapid SNM degradation when the bitlines' voltages are too low.

Kellah 06

The motivation of this paper is to use pulses to improve read stability. The paper claims great improvement using the pulsed bitline and wordline schemes with the read-modify-write scheme. By pulsing the bitline, you are able to reduce the voltage of the bitlines. By pulsing the wordline, you are able to turn of the access transistor before the bitcell has a read upset. Though the margin improves, there is a multiple cycle penalty added to each write or read operation and also increases the energy per operation.